MSAG®-LITE: GaAs IC PROCESS TECHNOLOGY ADDRESSING DEFENSE CONVERSION

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Abstract

In the mid 1980's the ITT Gallium Arsenide Technology Center (ITT GTC) developed a planar GaAs IC process based on ion implanted self aligned gate (SAG) FETs specifically for military applications [1, 2] With only one additional implant mask for each device type, high speed enhancement/depletion (E/D) digital, low noise microwave and high efficiency power microwave FETs could be fabricated on a single chip. Hence, the process was denoted Multifunction Self-Aligned Gate or MSAG®[3]. Recognizing the growing importance of commercial applications, ITT GTC launched a major effort in 1989 to tailor the MSAG® process for low frequency (<6 GHz) applications, by simplifying the process and lowering the costs associated with wafer fabrication and cycle time. This effort brought about the MSAG®-Switch process and later, MSAG®-Lite [4]. This paper explains how the process conversion took place, the applications that were targeted, and the products that resulted.

Introduction

The primary motivation for the development of the MSAG® process was to make highly integrated digital/MMIC chips a practical reality through improved manufacturability. Targeted applications were military systems such as Active Aperture Radar and Electronic Warfare (EW) [5, 6]. In 1989, the MSAG®-Switch process was developed for lower frequency commercial switch and control applications. Since these applications were at lower frequencies, and low cost was the primary driver, numerous process steps needed for higher frequency circuits were stripped out. In 1991, ITT GTC further developed the process in order to address additional commercial functions of radio front ends, such as receivers, mixers, and up/down converters, with low cost again being of primary importance. This resulted in the MSAG®-Lite process, which retained the full capability to address digital and microwave functions. Utilizing this process, ITT GTC announced several low cost RF IC power amplifiers for the rapidly expanding wireless communications market.

MSAG®-Switch

Although the high performance military-based GaAs technology (MSAG®) had provided an effective foundation for high volume applications, the costs associated with wafer production were still too high. The key to converting this technology to the commercial arena was to reduce or eliminate the high cost drivers of the process by developing subsets of the MSAG® process. The first process modification to benefit from these efforts was the MSAG®-Switch process.

This new process targeted the commercial need for low cost MMIC switch and control products. Since the MSAG® process was developed to enable high frequency power amplification, it contained features such as airbridges and through-wafer vias that were not necessary for RF switch circuits. Consequently, these features were eliminated in order to reduce the cost of the GaAs die area and manufacturing cycle time. Due to lower current density requirements, the 4.5 μm layer of gold plating (M2) was reduced to 1.0 μm evaporated gold. The first metal (M1), which was used as a local interconnect for low gate resistance for power amplification, was unnecessary and was eliminated. Finally, the process was streamlined by using blanket channel and n^+ implants. In total, the process was reduced from 50 major operations to 30. Only six photomasks were required for MSAG®-Switch compared to twelve for MSAG®.

In addition to shortening manufacturing cycle time, component costs were reduced using concurrent engineering techniques to optimize the SAG FET's RF performance and maximize circuit yields. Key transistor specifications such as on-resistance (R_{ON}), breakdown voltage (BV_{GDO}), and threshold voltage (V_T) were derived from competitive switch performance specifications such as insertion loss, isolation, and RF power handling. Based on these specifications, two switch FETs were initially

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developed for operation with 3 V and 5 V systems supplies. In SAG technology, R_{ON} and BV_{GDO} are varied by adjusting the distance (L_{GD}) between the gate and the n^+ region. In doing so, these two important FET parameters are traded off against one another. The chosen L_{GD} dimension was centered within the desired region of both parameters in order to maximize the yield of each.

The final modification to the MSAG® process involved the protection of the die from the plastic packaging process, which was necessary for compatibility with the high volume plastic surface mount technology used for silicon ICs. This was accomplished with the addition of a SiON dielectric scratch protection layer over the entire wafer, which protected the circuitry and aided in assembly yield.

Upon completion of the MSAG® process conversion to MSAG®-Switch, the goals of shorter wafer cycle time, higher yield, and reduced cost were achieved. For standard priority wafers, the cycle time was reduced from seven weeks to 3.5 weeks. Due to the transistor optimization and uniformity, the overall wafer yield for the new process in 1993 was better than 85% [4]. These improvements reduced wafer costs by 50% and enabled ITT GTC and Alpha Industries to develop a highly competitive RF switch product line. To date, 10 million packaged GaAs chips have been sold at prices from a few dollars to less than one dollar, where prices had previously averaged $15.00.

MSAG®-Lite

Building on the success of MSAG®-Switch, ITT GTC further developed the MSAG® process to address a broader range of RF IC functions for commercial applications. The first change to the MSAG®-Switch process in developing MSAG®-Lite was to reinstate the use of the first metal M1, in order to bring back the low gate resistance for power amplification. Although the initial plans were to retain the 1.0 µm evaporated gold for the top metal layer M2, it contributed to lossy inductors (Q<10 @ 900MHz) and unusually large FET geometries needed to handle the higher currents associated with power amplifiers. In order to avoid these problems, the 4.5 µm gold plating used on MSAG® was reinstated. This change enabled smaller FET designs and increased the inductor Q's by a factor of 2. Table I summarizes the major differences between the three ITT GTC fabrication processes [4].

Due to the high volumes associated with the targeted wireless applications (millions of units per month), the goal for the commercialized GaAs process and its products, was to utilize the techniques and processes used in the Silicon-based semiconductor industry in as many ways possible. This approach would insure that ITT GTC's products would not need any special handling, assembly techniques, or implementation. This was accomplished with the selection of the 16 pin narrow body SOIC package and the addition of the glassivation layer for circuit scratch protection. As a result of these

Feature	MSAG®	Lite	Switch
Frequency (GHz)	<20	<6	<6
V_{DD} (V)	5 to 9	1.5 to 7	3 to 5
M1 (µm)	0.6	0.6	none
M2 (µm)	4.5	4.5	1.0
Glassivation	polyimide	polyimide	SiON
Airbridges	yes	no	no
Through-wafer Vias	yes	no	no
Photo-ops	12	8	6
Total ops	50	37	30

Table I. Features of the dual use MSAG® processes.

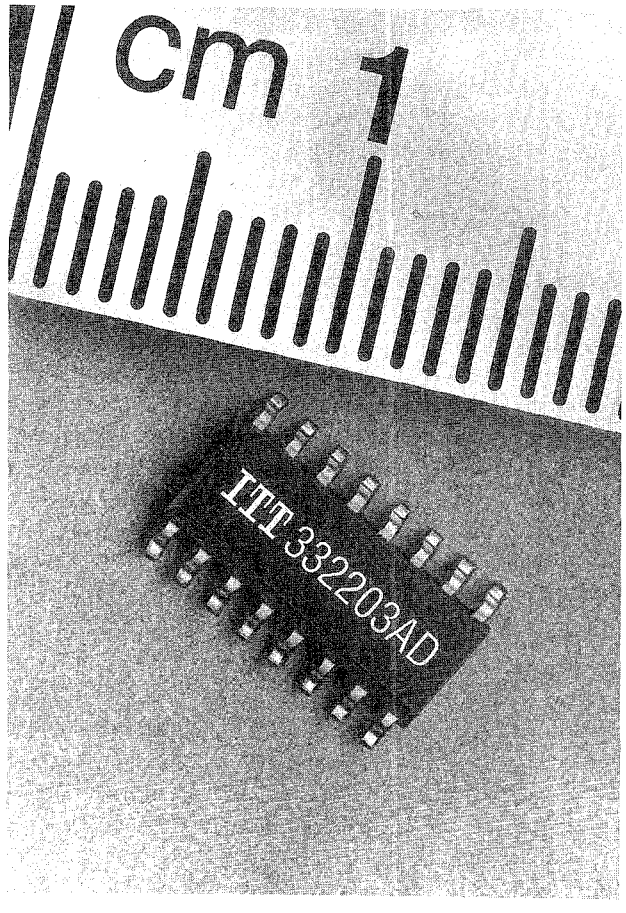

Figure 1. RF Power Amplifier in a 30 mm² SOIC Plastic Package.

measures, the packaging method for ITT GTC's RF ICs is an industry standard outline for high volume manufacturing and use by customers in the wireless communications industry. An example of the RF IC package is shown in Figure 1.

When addressing the need for a glassivation layer in the MSAG®-Lite process, the SiON layer used in the MSAG®-Switch process could not be used due to the increased thickness of the top metal. Instead, a thicker polyimide dielectric (ε_r=3.1) was used to cover the 4.5 μm gold layer.

Finally, with the initial emphasis on power amplifier IC's, the FETs themselves had to be optimized for good power added efficiency (PAE), which is essential for long battery life in wireless systems. In addition to the DC bias voltage, there are four key FET parameters that define the operating load line, compression, and linearity of the amplifier. Thus there were several considerations in designing the FETs. FET parameters such as peak current (I_{PEAK}), breakdown voltage (BV_{GDO}), knee voltage (V_K), and threshold voltage (V_T) were chosen to enable the FET to deliver the desired power with maximum efficiency, while maintaining the advantage of small size and low cost. Using these criteria, two power FETs were developed for the MSAG®-Lite process that targeted 3.6 V and 6 V system supplies.

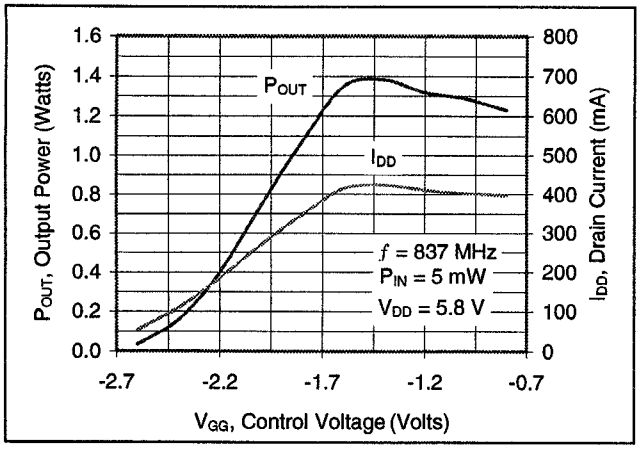

Figure 2: Typical P_{OUT} and I_{DD} vs. V_{GG} for ITT334103BD Power Amplifier RF IC.

The FET design for 6 Volt applications was denoted as SF3. This FET was basically the 3 V switch FET with doping modifications. The goal was to achieve a high P_{1dB} power to gate periphery (mW/mm) ratio with a 6 V supply while providing greater than 50% PAE [7]. Being a depletion mode type FET, the SF3 transistor requires a negative gate bias. This added degree of freedom enables Class AB operation of the FET. In addition to higher efficiency, this capability provides a means of output power control and a method to save battery current under backed-off power conditions. This is shown in Figure 2, which plots the typical power out and drain current of a 5.8 Volt power amplifier IC as a function of gate voltage (control voltage).

The product represented in Figure 2, is one of three amplifier RF ICs that ITT GTC has released for the Advanced Mobile Phone Service (AMPS) frequency band (824-849 MHz) using this FET type in the MSAG®-Lite process. ITT GTC is currently developing products for ISM, ETACS, and GSM applications as well. The characteristic performance of three AMPS products is shown in Table II.

Part No.	V_{DD}	Pout	PAE
ITT333101BD	4.6 V	1.0 W	58 %
ITT334102BD	5.8 V	1.0 W	55%
ITT334103BD	5.8 V	1.2 W	55%

Table II: MSAG®-Lite Power Amplifier RF ICs for AMPS Utilizing SF3 Transistors

The MSAG®-Lite FET design for 3 V supplies, titled SF1 [8], was transferred over from the MSAG® process due to its low noise figure (<1 dB @ 2 GHz). In addition to the capability of using this FET for low noise amplifiers, it could also be effectively operated with a single supply voltage [9, 10]. Since I_{DSS} of this FET is roughly 50% of I_{PEAK}, Class A operation can be achieved with grounded gates. This is highly desirable in the wireless communications market since additional circuitry to generate a negative supply voltage is not necessary. In order to increase power added efficiency, the FETs are operated in compression. A comparison of the SF1 and SF3 FETs is shown in Table III [4]. Accelerated life testing has been performed on these FET designs, showing excellent mean time to failure (MTTF) of $>10^8$ hours at T_J=150 °C [11].

Feature	SF1	SF3
Typical V_{DD} (V)	3.3	4.6, 5.8
f_t (GHz)	19	17.5
P_{1dB} (mW/mm)	200	250
MAG @ 2 GHz (dB)	18	12
I_{PEAK} (mA/mm)	300	330
I_{DSS} (mA/mm)	155	220
V_K @ 0.7 V_{GS} (V)	1.0	1.5
V_T (V)	-0.95	-1.6
BV_{GDO} @ 1mA/mm (V)	8	17

Table III. MSAG®-Lite power FET characteristics.

Using the SF1 FET design in the MSAG®-Lite process, ITT GTC has released two low cost 3 V RF IC power amplifiers, one for two-way paging applications (890-940 MHz), and one for the Digital European Cordless Telephone (DECT), which operates at 1.9 GHz. The characteristic performance of these products is shown in Table IV.

Part Number	Application	V_{DD}	P_{OUT}	PAE
ITT332102BD	ISM/Paging	3.3 V	1.1W	35 %
ITT332202AD	DECT	3.6 V	0.4W	25 %

Table IV: MSAG®-Lite Power Amplifier RF ICs Utilizing SF1 Transistors

In order to integrate power amplifiers and LNAs with other front-end radio functions, such as mixers and up/down converters, the E/D digital process used in MSAG® was carried over to the MSAG®-Lite process. Due to the nature of the implant method used in the SAG process, all of these FET types can be readily fabricated on the same wafer. ITT GTC will soon be developing multifunctional RF ICs that will continue to provide small size and low cost advantages in the commercial market due to the ease of integration and resulting high RF yield.

Conclusion

The MSAG® process was specifically developed for military applications. Over the last several years, this technology and its applications have been greatly accelerated. As a result, several ITT GTC military programs are moving forward towards production. This paper has described how ITT GTC has actively pursued the dual use of its GaAs MMIC process by developing two streamlined versions called MSAG®-Switch and MSAG®-Lite. These processes were driven by commercial market requirements for small size, low cost, and quick time-to-market. Due to the fact that these applications required lower supply voltages, lower frequencies, and lower output powers, it was possible to eliminate several process steps in the MSAG® process which were required for higher frequency and higher power applications. Although a few steps were added back to the MSAG®-Switch process in developing MSAG®-Lite, the advantage of low cycle time and reduced chip costs was retained. Thus MSAG®-Lite is a good example of how a high performance military technology can be adapted to serve a high-volume low-cost commercial market by optimizing key performance requirements against a strict set of cost criteria.

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